REMARKS

Applicant elected to prosecute claims 1-10 and 25-44 (Group I claims) as a result of the election requirement dated June 23, 2005, therefore, claims 1-10 and 25-44 are pending in the present application.

The Examiner rejected claims 1-10 and 25-44 under 35 U.S.C. 112, as being indefinite. In light of the Amendments and arguments provided herein, Applicant respectfully asserts that the rejections under 35 U.S.C. 112 are now moot, and that claims 1-10 and 25-44 are allowable.

Regarding Examiner's rejections of claims 1, 25 and 35, the Examiner stated that there are no means to perform the switching function recited in the claims. Applicant respectfully disagrees. For example, claim 1 clearly recites a "delay circuit" for switching and activation of a capacitive delay. The delay circuit provides for switching the activation of the capacity delay using a switch. Likewise, claims 25 and 35, both as amended, also call for delay circuit for switching an activation of the capacitive delay using a switch. Therefore, the Examiner's rejection of claims 1, 25 and 35, under 35 U.S.C. § 112 is now moot and Applicant respectfully asserts that claims 1, 25 and 35 are allowable.

Regarding the rejections of claims 4, 28 and 37, the rejections under § 112 are now moot. Claims 4, 28 and 37, as amended, call for a phase detector to detect said phase difference, which is indeed clear as to the phase detector detecting the phase difference. Further, although Applicant disagrees that the course delay, fine delay, and phase delay lacks connectivity since they are clearly called for being included in the delay block loop. Claims 4, 28 and 37 (as amended) the feedback delay unit calls for operatively being coupled to the course delay unit, the find delay unit, and the phase detector unit. Therefore, the rejections of claims 4, 28, and 37

under 35 U.S.C. § 112 are now moot and Applicant respectfully asserts that claims 4, 28, and 37 are allowable.

Regarding claims 5, 29, and 39, Applicant respectfully disagrees that the first inverter, transistors and the second inverters are not connected properly. The first inverter, transistors and the second inverters are part of the fine delay unit and their connections are readily deciphered by those skilled in the art. Accordingly, Applicant respectfully asserts that claims 5, 29, and 39 are allowable.

Regarding claims 6-7, 30-31, and 40-41, amendments have been made to correct typographical errors and to address the Examiner's concerns. In light of the amendments made to claims 6-7, 30-31, and 40-41, the rejections of claims 6-7, 30-31, and 40-41 under 35 U.S.C. § 112 are now moot and Applicant respectfully asserts that claims 6-7, 30-31, and 40-41 are allowable.

Regarding Examiner's assertion that in claims 8, 32, and 42, the "N-channel" and "P-channel" transistors sets are not read on preferred embodiment, the Applicant respectfully disagrees. These terms are adequately described in the specification and reference numbers are provided to reference them in the drawings (for example, see Specification, Page 17, lines 13-17; Page 18, lines 8-11, and Figure 5). The terms "N-channel" and "P-channel" transistors sets would be clear to those skilled in the art since they are adequately described in the Specification and in the Drawings, and are recited clearly in claims 8, 32, and 42. The rejections of claims 8, 32, and 42 under 35 U.S.C. § 112 are now moot and Applicant respectfully asserts that claims 8, 32, and 42 are allowable.

Regarding claims 9, 33, and 34, amendments have been made to claims 9, 33, and 34. In light of the amendments to claims 9, 33, and 34, all antecedent issues have been addressed. Hence, rejections of claims 9, 33, and 34 under 35 U.S.C. § 112 are now moot and Applicant respectfully asserts that claims 9, 33, and 34 are allowable.

Regarding claim 25, the Examiner expressed questions as to how data could be stored in a memory location. Applicant respectfully directs the Examiner's attention to line 2 of claim 25, which recites a "first device" the comprises a "memory location", in which data may be stored. It would be readily clear to those skilled in the art that the memory location in the first device would be capable of storing data. Amendments have be made to claim 25 to address the Examiner's other concerns regarding claim 21. Hence, rejections of claim 25 under 35 U.S.C. § 112 are now moot and Applicant respectfully asserts that claims 25 is allowable.

In light of the amendments and arguments provided herein, the rejections of claims 1-10 and 25-44 under 35 U.S.C. § 112 are now moot and Applicant respectfully asserts that claims 1-10 and 25-44 are allowable.

Claims 1-4, 9-10, 35-38 and 43-44 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,327,318 ***(Bhullar)***. In light of the amendments and arguments provided herein, Applicant respectfully traverses this rejection.

Applicant respectfully asserts that ***Bhullar*** does not teach, disclose or suggest all of the elements of claims 1 and 35 of the present invention. The Examiner relies upon the disclosure in ***Bhullar*** to read upon the delay circuit for switching an activation of a capacitance using a switch, as called for by the amended claims 1 and 35 of the present invention. However, ***Bhullar*** does not disclose switching an activation of the capacitor delay using a switch. The Examiner

cited Figure 2 of ***Bhullar*** to read upon claims 1 and 35. However, it is clear that ***Bhullar***, in Figure 2, merely discloses a plurality of capacitors 21 that are selectable by binary logic signal outputs from a thermometer decoder 11. In contrast, claims 1 and 35 call for a delay circuit for switching an activation of a capacitive delay using a switch. ***Bhullar*** does not disclose switching an activation of the capacitor delay using a switch. ***Bhullar*** merely discloses that the thermometer decoder may select any of five binary weighted capacitors based upon a five-bit logic signal, which refers is a control of one bit per capacitor. *See* column 4, line 30-41, Figure 2. However, claims 1 and 35 call for switching the activation of the capacitor delay using a switch, which is not taught, disclosed or suggested by ***Bhullar***. For at least these reasons, independent claims 1 and 35, as amended, are not taught, disclosed or suggested by ***Bhullar*** and therefore, are allowable.

Claims 1 and 35 provide for novelty that overcomes weaknesses in prior art systems such as ***Bhullar***. Direct control of modifying capacitance is implemented by the present invention, which may provide advantages such as a reduction of the need for multiplexer to implement or exclude capacitive multiplexers. This has the advantage of overcoming the resistor interferences caused by a multiplexer, such as modification of the RC time constant caused by the resistivity of the multiplexer. Therefore, the switching of the activation of the capacitance called for by claims 1 and 35 clearly provides an advantage as exemplified by the exemplified advantages disclosed in the specification. *See,* Specification page 9, lines 10-10. The cited prior art do not disclose the switching of the activation of the capacitor delay using a switch, and therefore, do not provide the advantages of the present invention. Since the cited prior art do not disclose the switching of the activation of the capacitor delay using a switch, claims 1 and 35 are not taught, disclosed, or suggested by the prior art.

Claims 5-8 and 39-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Bhullar*** in view of U.S. Patent No. 6,700,434 ***(Fujii)***. In light of the amendments and arguments provided herein, Applicant respectfully traverses this rejection.

Applicant respectfully asserts that the combination of ***Bhullar*** and ***Bhullar*** do not make obvious all of the elements of the claims of the present invention. The Examiner cited ***Fujii*** to make up for the deficit of ***Bhullar*** regarding claims 5-8 and 39-42. However, Applicant respectfully asserts that ***Fujii*** does not supply the elements that are missing in the disclosure of ***Bhullar***.

Firstly, ***Bhullar*** clearly does not disclose the underlying elements of switching the activation of the capacitance delay using a switch in a delay lock loop, which are called for by claims 5-8 and 39-42 by the virtue of their dependencies. Adding the disclosure of ***Fujii*** does not make up for this deficit. ***Fujii*** merely discloses a bias voltage generating circuitry where a selector selects outputs of multiple plurality of isolation outputs to provide a substrate bias voltage. Secondly, the Examiner is merely using disclosures of NMOS and PMOS transistors on the output of a ring isolator 10 that is directed to controlling a PMOS and an NMOS transistor, to read upon the N-channel and P-channel transistor sets utilized in performing the switching of an activation of the capacitive delay in a delay lock loop, as called for by claim 5 and 39.

Applicant respectfully asserts that the Examiner uses improper hindsight reasoning to pick and choose disclosure of NMOS and PMOS transistors to apply this disclosure to the delay lock loop disclosure of ***Bhullar***. However, even when combining ***Bhullar*** and ***Fujii***, the mere disclosure of the ring oscillator turning the PMOS transistor and the NMOS transistor to add a gate-capacitance of the PMOS transistor, does not make obvious the elements of the N-Channel

transistor set and the P-Channel transistor set being utilized for performing the switching of the activation of the capacitor delay using a switch in a delay lock loop, as called for by claims 5-8 and 39-42 of the present invention. Additionally, Applicant respectfully assert without using hindsight reasoning, those skilled in the art would not combine the bias voltage generating circuit with the delay lock loop of disclosure of ***Bhullar*** to make obvious all of the elements of claim 1 of the present invention.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. As described above, the combination of ***Bhullar*** and ***Fujii*** do not teach or suggest all of the elements of claims 5-8 and 39-42 of the present invention.

Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Applicant respectfully asserts that the Examiner has provided no evidence nor any evidence in the cited prior art that would provide an indication of motivation of those skilled in the art to combine ***Bhullar*** and ***Fujii*** to read upon all of the elements of claims 5-8, 39-42 of the present invention. Without improper hindsight, those skilled in the art simply would not find the motivation to combine the bias voltage generating circuit of ***Fujii*** with the delay of locked loop circuit of ***Bhullar***. Therefore, there is no evidence or motivation, either in the references themselves or in the knowledge, generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings.

Third, there must be a reasonable expectation of success. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in

the prior art, and not based on appellant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142. There is no evidence that the improbable combination of ***Bhullar*** and ***Fujii*** provide a reasonable expectation of success. There is no evidence to the contrary and the Examiner fails to provide any evidence of reasonable expectation of success based upon the prior art. Therefore, the Examiner failed to establish a *prima facie* evidence of obviousness with respect to claims 5-8 and 39-42 of the present invention. Accordingly, for a least the reasons described above ***Bhullar*** and ***Fujii*** do not cause all of the elements of claims 5-8 and 39-42 to be are taught, disclosed, or suggested. Accordingly claims 5-8 and 39-42 are allowable.

Claims 25-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,323,705 ***(Shieh)***, in view of ***Bhullar*** and further in view of ***Fujii***. In light of the amendments and arguments provided herein, Applicant respectfully traverses this rejection.

The Examiner combines the disclosure of ***Shieh*** with the disclosures of ***Bhullar*** and ***Fujii*** to reject claims 25-34 of the present invention. However, neither ***Bhullar*** nor ***Fujii*** disclose a delay lock loop comprising a delay circuit for switching an activation of the capacitor delay using a switch, as called for by claim 25 of the present invention. Presumably, the Examiner cited ***Shieh*** for disclosing the second device coupled to the memory for accessing data. However, as the Examiner admitted on page 6 of the Office Action dated August 5, 2005, ***Shieh*** does not disclose a delay lock loop comprising a delay circuit for switching and activation of the capacitor delay, as called for the by claim 25 of the present invention.

Further, as described above, ***Bhullar*** simply does not disclose the activation of the capacitor delay using a switch as called for by claim 25 of the present invention. Additionally,

the bias voltage generation circuit of ***Fujii*** does not make up for the deficit of ***Shieh*** and ***Bhullar***. Therefore, adding the disclosure of ***Shieh*** does not make obvious all of the elements of claim 25 of the present invention. As described above, those skilled in the art would not find motivation without improper hindsight reasoning to combine the bias voltage disclosure of ***Fujii*** with the delay lock loop disclosure of ***Bhullar***.

Further, the delay circuitry of ***Shieh*** merely is directed to utilizing shift registers for performing delay shift registers. Those skilled in the art would not make obvious all of the elements by combining ***Shieh*** with ***Bhullar*** to make obvious all of the elements of claim 25 of the present invention and as provided above. Simply because ***Shieh*** discloses a ring oscillator controlling a PMOS oscillator and turning on an NMOS transistor or a PMOS transistor to add delay amounts does not provide subject matter that would make obvious all of the elements of claim 25. Such bias voltage generation simply is not combinable with ***Shieh*** or ***Bhullar***, without using improper hindsight reasoning, since the cited prior lacks sufficient motivation to combine ***Shieh***, ***Bhullar***, and/or ***Fujii***. Adding ***Shieh*** would simply not disclose switching an activation of capacitor delay simply does not make up for the deficit of the prior art. Therefore, the Examiner has failed to provide that the combination of ***Shieh***, ***Bhullar***, and/or ***Fujii*** would make obvious all of the elements of claim 25 of the present invention. Also, the Examiner had failed to show that there is sufficient motivation to combine ***Shieh***, ***Bhullar***, and/or ***Fujii*** to make obvious all of the elements of claim 25 of the present invention. Additionally, the Examiner failed to show that there would be a reasonable expectation of success in combining ***Shieh***, ***Bhullar***, and/or ***Fujii***. In fact, as described above, those skilled in the art would not combine ***Shieh***, ***Bhullar***, and/or ***Fujii***. Without using improper hindsight reasoning. Therefore, the Examiner failed to establish a *prima facie* evidence of obviousness with respect to claim 25 of

the present invention. Accordingly, for a least the reasons described above ***Shieh***, ***Bhullar***, and/or ***Fujii***. do not cause all of the elements of claim 25 to be are taught, disclosed, or suggested. Accordingly claim 25 of the present invention is allowable for at least the reasons cited herein. Additionally, claims 26-34, which depend from independent claim 25 are also allowable for at least the reasons cited above.

Reconsideration of the present application is respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Houston, Texas, telephone number (713) 934-4069 to discuss the steps necessary for placing the application in condition for allowance.

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